Abstract

METHOD AND APPARATUS FOR MEASUREMENT OF JITTER

A method and circuit for measurement of jitter in which a reference clock (404) runs at a frequency offset to the incoming signal (I) so that the phase of the two clocks drift over time, enabling detection of jitter in the input signal by measurement of the difference in the number of clock cycles it takes for this drift to occur.

This design provides the following advantages:

- It does not require analogue circuitry and, because the frequency offset can be large and still function, the reference frequency can be produced by a programmable oscillator.
- With the exception of the programmable oscillator the entire design can be implemented within an FPGA.
- It requires no parts (such as a jitter attenuator or phase locked loop) designed to operate at a specific frequency and therefore this design can operate over an extremely wide frequency range.